AMENDMENTS TO THE DRAWINGS:

FIG. 9 has been amended to replace "$j \geq k$" with "$k > j$" at step S13. Corresponding to the amendments made in the specification at page 18, the paragraph beginning at line 12.

REMARKS

Minor amendments have been made to the specification and FIG. 9. Also, claims 1, 3, 4, 7 and 8 have been amended. Support for the claim amendments can be found at FIG. 6. Claims 1-4 and 7-8 are pending and under consideration. Reconsideration is respectfully requested.

I. REJECTION OF CLAIMS 1, 2, 7 AND 8 UNDER 35 U.S.C. § 101:

Claims 1, 7 and 8 have been amended to overcome the rejection.

II. REJECTION OF CLAIMS 1-4 UNDER 35 U.S.C. § 103(a) AS BEING UNPATENTABLE OVER KAMETANI (previously cited) IN VIEW OF LEWIS (previously cited):

At page 4 of the Office Action, the Examiner admits Kametani fails to disclose all of the features recited in claim 1. However, the Examiner asserts that Lewis makes up for the deficiencies of Kametani at in the Abstract and column 9, line 60 – column 10, line 40.

The Applicants respectfully submit that neither Kametani nor Lewis, individually or combined, disclose all of the features recited in amended claim 1, for example.

That is, neither of the foregoing references disclose "providing a parallel processing control information region indicating a first parallel processing block number, providing, for each of the plurality of threads, a thread information region indicating a second parallel processing block number, providing a parallel processing block control information region containing an executed thread number, causing each processor to increment the second parallel processing block number of the thread information region corresponding thereto when said each processor has finished a current parallel processing block and, when the incremented second parallel processing block number exceeds the first parallel processing block number, causing each processor to update the first parallel processing block number accordingly and creating a new parallel processing block control information region corresponding to the updated first parallel processing block number, and causing each processor to increment the executed thread number in the corresponding parallel processing block control information region when said each processor has finished a current parallel processing block thereof, and causing said each processor to delete the parallel processing block control information region when the incremented executed thread number equals a total number of threads," as recited in amended claim 1.

Instead, column 10, lines 1-40 of Lewis merely discloses if a thread is available to process a block in accordance with its specified program code, the thread determines whether there are any blocks in the queue, and if so, the available thread selects a block fro the queue for processing. However, if a thread determines that a selected block is dependent upon the execution of program code with respect to other blocks that have not been executed, the thread skips the selected block. Otherwise, if any block dependencies have been satisfied, the thread uses an assigned processor to execute the program code associated with the block. Further, a thread may skip processing blocks in the queue and continue to process other queued blocks depending upon the dependency relationships associated with each block in the queue.

However, Lewis does not discloses any details regarding synchronization between the threads. Instead, Lewis only discloses a thread being able to skip processing blocks in a queue and proceed to other queued blocks based upon the dependency relationships of each block.

Thus, various claims of the present invention provide details regarding the status of each thread and the synchronization between each thread. For example, amended claim 1 recites "causing each processor to increment the second parallel processing block number of the thread information region corresponding thereto when said each processor has finished a current parallel processing block and, when the incremented second parallel processing block number exceeds the first parallel processing block number, causing each processor to update the first parallel processing block number accordingly and creating a new parallel processing block control information region corresponding to the updated first parallel processing block number, and causing each processor to increment the executed thread number in the corresponding parallel processing block control information region when said each processor has finished a current parallel processing block thereof, and causing said each processor to delete the parallel processing block control information region when the incremented executed thread number equals a total number of threads".

Therefore, the combination of Kametani and Lewis fails to establish a prima facie case of obviousness over the present invention. Thus, it is respectfully submitted that the rejection is overcome.

Although the above comments are specifically directed to claim 1, it is respectfully submitted that the comments would be helpful in understanding differences of various other rejected claims over the cited reference. Therefore, it is respectfully submitted that the rejection is overcome.

III. REJECTION OF CLAIMS 7 AND 8 UNDER 35 U.S.C. § 102(e) AS BEING ANTICIPATED BY LEWIS:

Claims 7 and 8 have been amended to recite similar features as those of amended claim 1. Therefore, the comments recited above in section II, may be applied here also.

IV. CONCLUSION:

In view of the foregoing amendments and remarks, it is respectfully submitted that each of the claims patentably distinguishes over the prior art, and therefore, defines allowable subject matter. A prompt and favorable reconsideration of the rejection along with an indication of allowability of all pending claims are therefore respectfully requested.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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